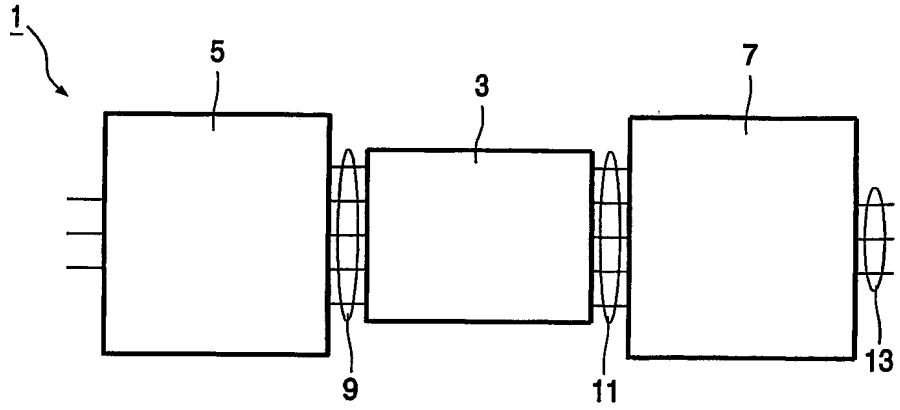

FIG. 1

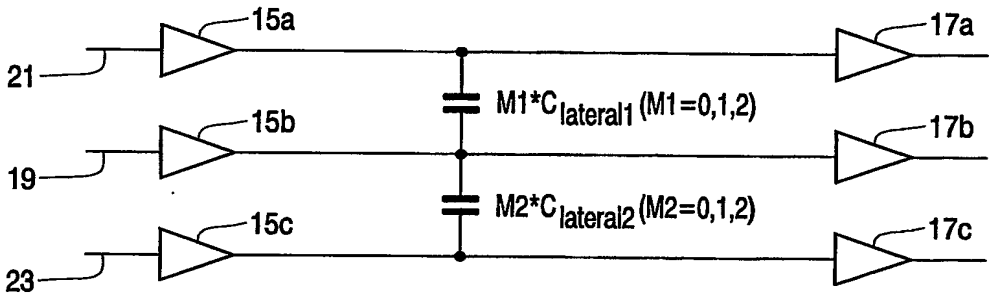

FIG. 2

Mode	Aggressor1	Victim	Aggressor2	Relative power (proportional to switched total capacitance)
Fastest (speed-up)	0 → 1	0 → 1	0 → 1	$C_{vertical}$ (including fringe)
Faster	0 → 1 Quiet	0 → 1 0 → 1	Quiet 0 → 1	$C_{vertical} + 1 * C_{lateral}$
Nominal	0 → 1 Quiet 1 → 0	0 → 1 0 → 1 0 → 1	1 → 0 Quiet 0 → 1	$C_{vertical} + 2 * C_{lateral}$
Slower	1 → 0 Quiet	0 → 1 0 → 1	Quiet 1 → 0	$C_{vertical} + 3 * C_{lateral}$
Slowest (slow-down)	1 → 0		1 → 0	$C_{vertical} + 4 * C_{lateral}$

FIG. 3

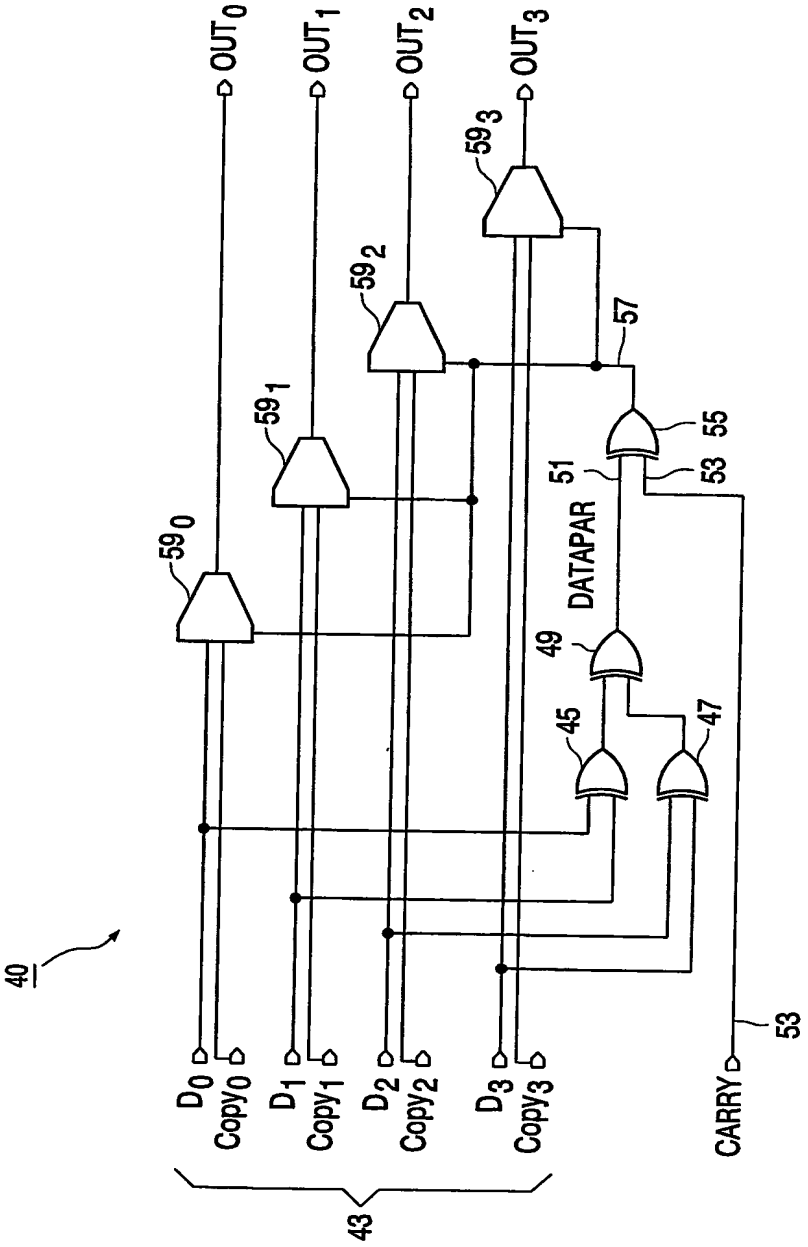
OUT0
OUT1
OUT2
OUT3
59 3
59 2
59 1
59 0
57
55
53
51
DATAPAR
49
45
47
40
D0
Copy0
D1
Copy1
D2
Copy2
D3
Copy3
43
CARRY
53

FIG. 4

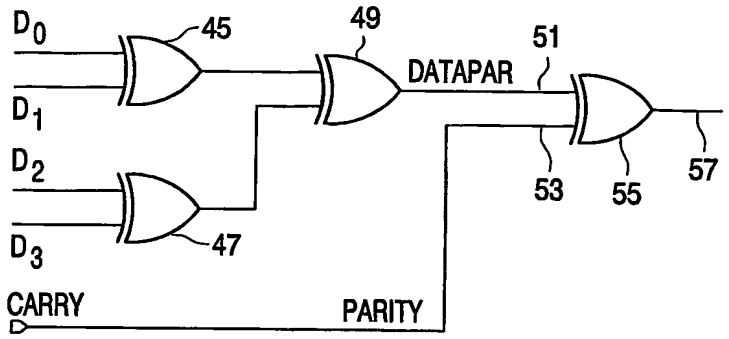
D0
D1
D2
D3
45
47
49
DATAPAR
51
53
55
57
CARRY
PARITY

FIG. 5

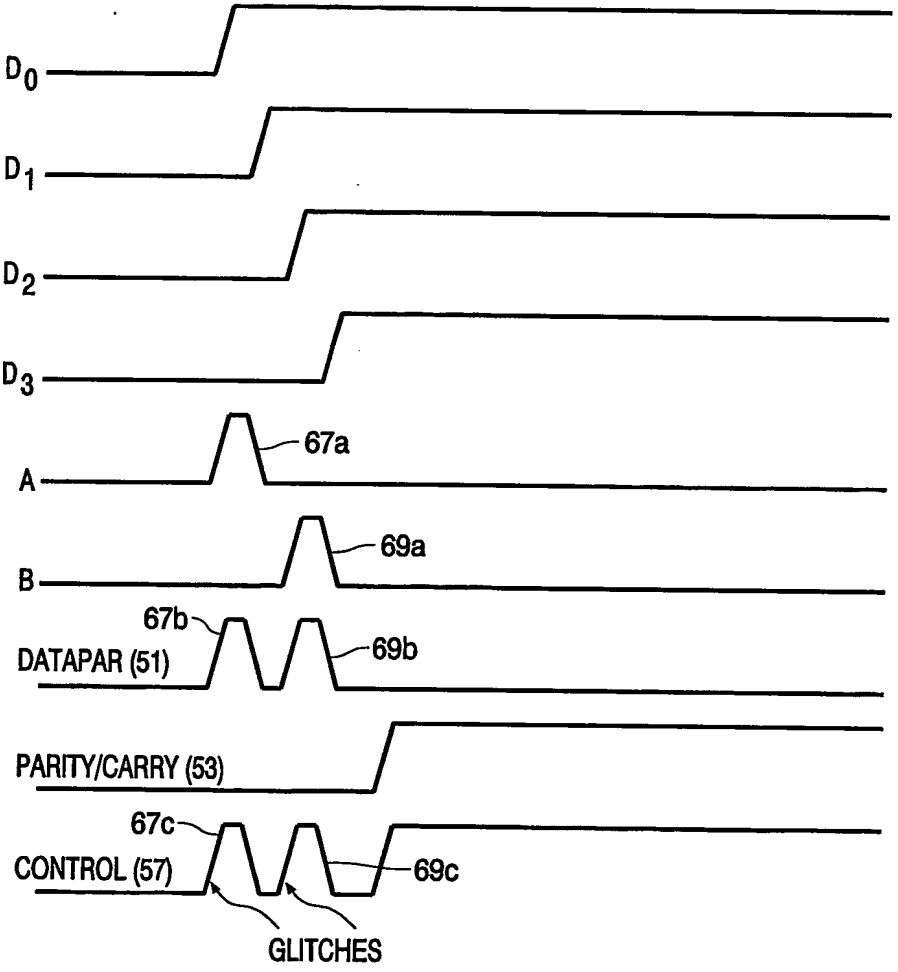
D0
D1
D2
D3
A
67a
B
69a
67b
DATAPAR (51)
69b
PARITY/CARRY (53)
67c
CONTROL (57)
69c
GLITCHES

FIG. 6

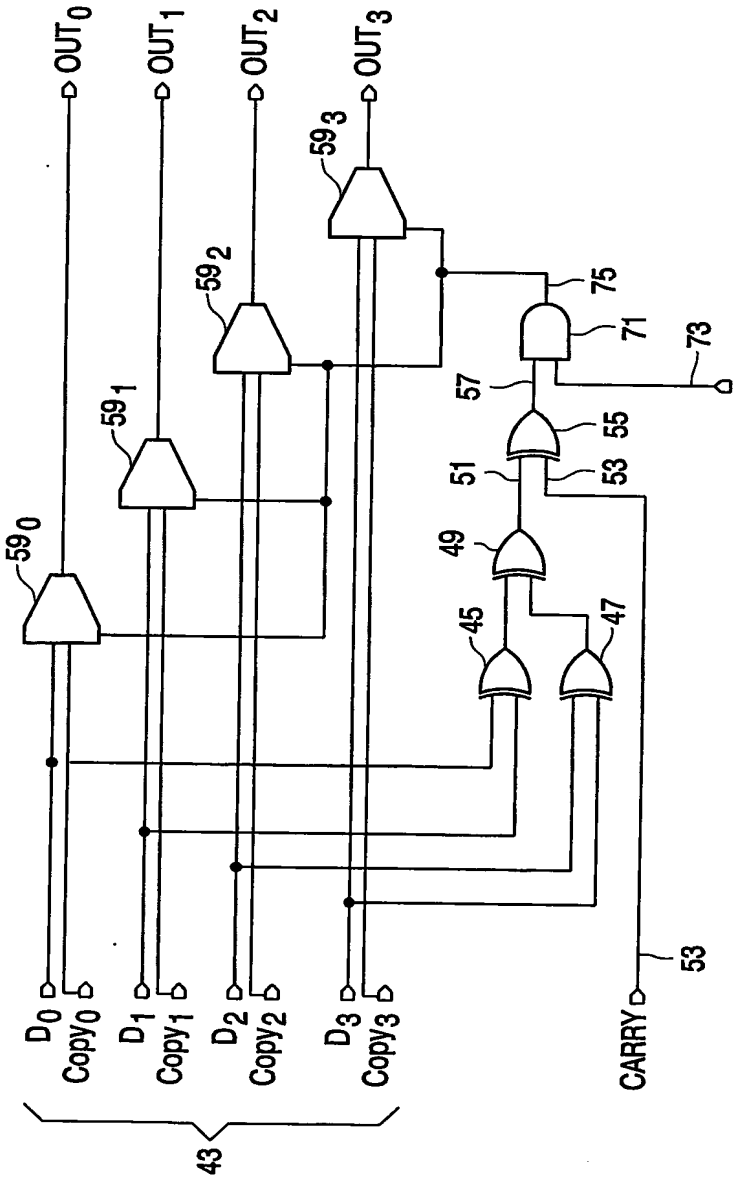
OUT0
OUT1
OUT2
OUT3
59 3
59 2
59 1
59 0
75
71
73
57
55
51
53
49
45
47
D0
Copy0
D1
Copy1
D2
Copy2
D3
Copy3
CARRY
53
43

FIG. 7

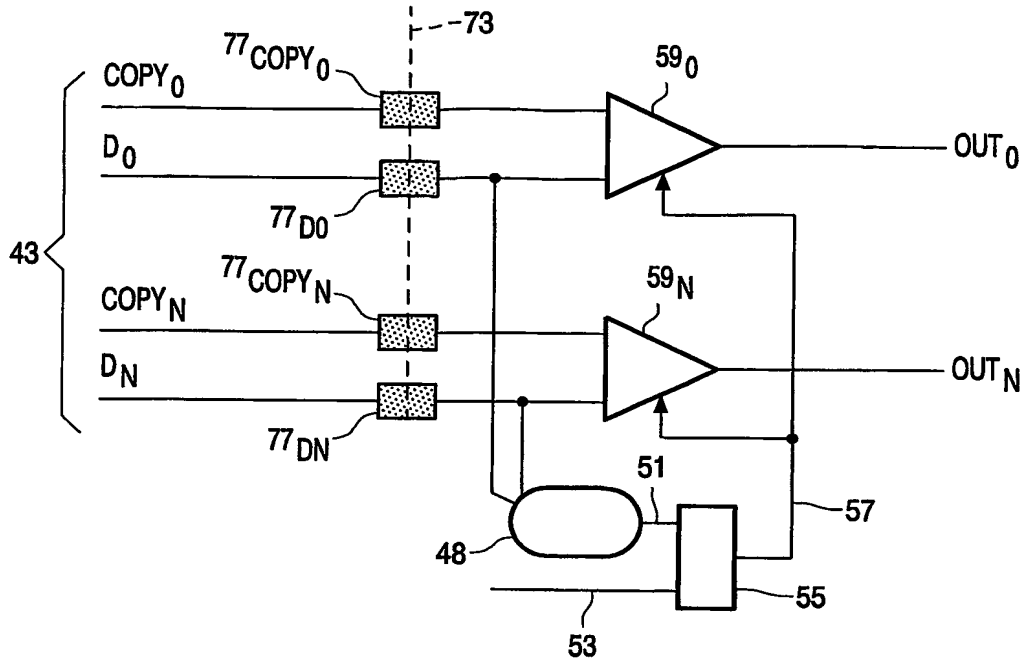
73
77COPY0
COPY0
D0
77D0
43
77COPYN
COPYN
DN
77DN
590
59N
OUT0
OUTN
51
57
48
55
53

FIG. 8

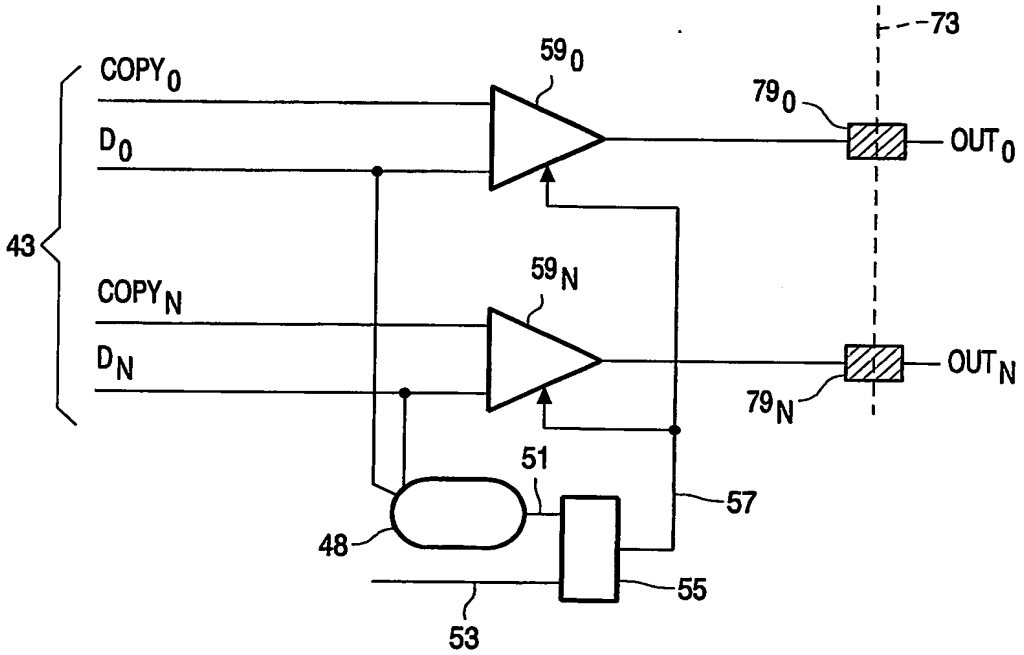
73
590
COPY0
D0
790
OUT0
43
59N
COPYN
DN
OUTN
79N
51
57
48
55
53

FIG. 9

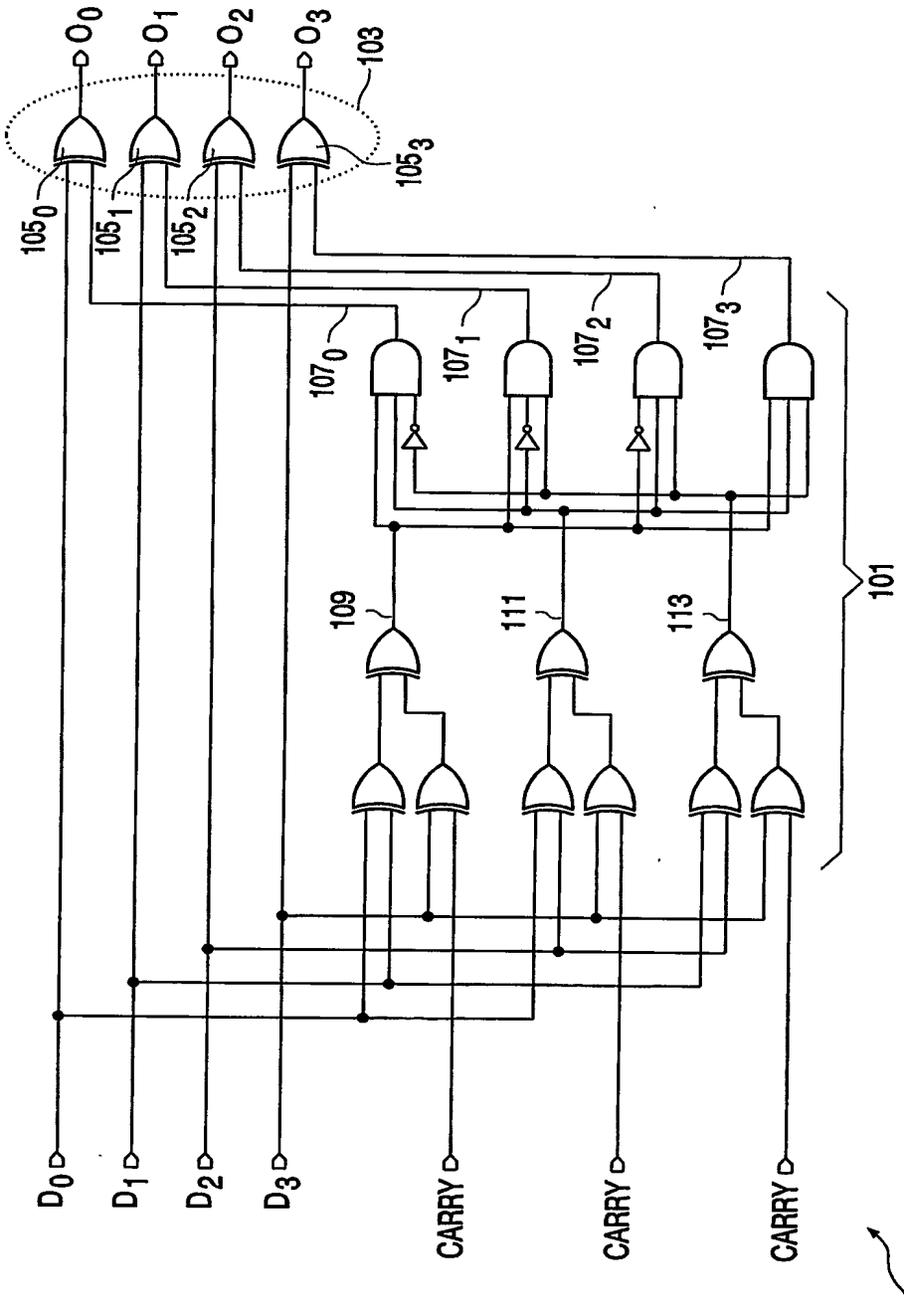
O0
O1
O2
O3
103
1053
1050
1051
1052
1070
1071
1072
1073
109
111
113
101
D0
D1
D2
D3
CARRY
CARRY
CARRY
100

FIG. 10

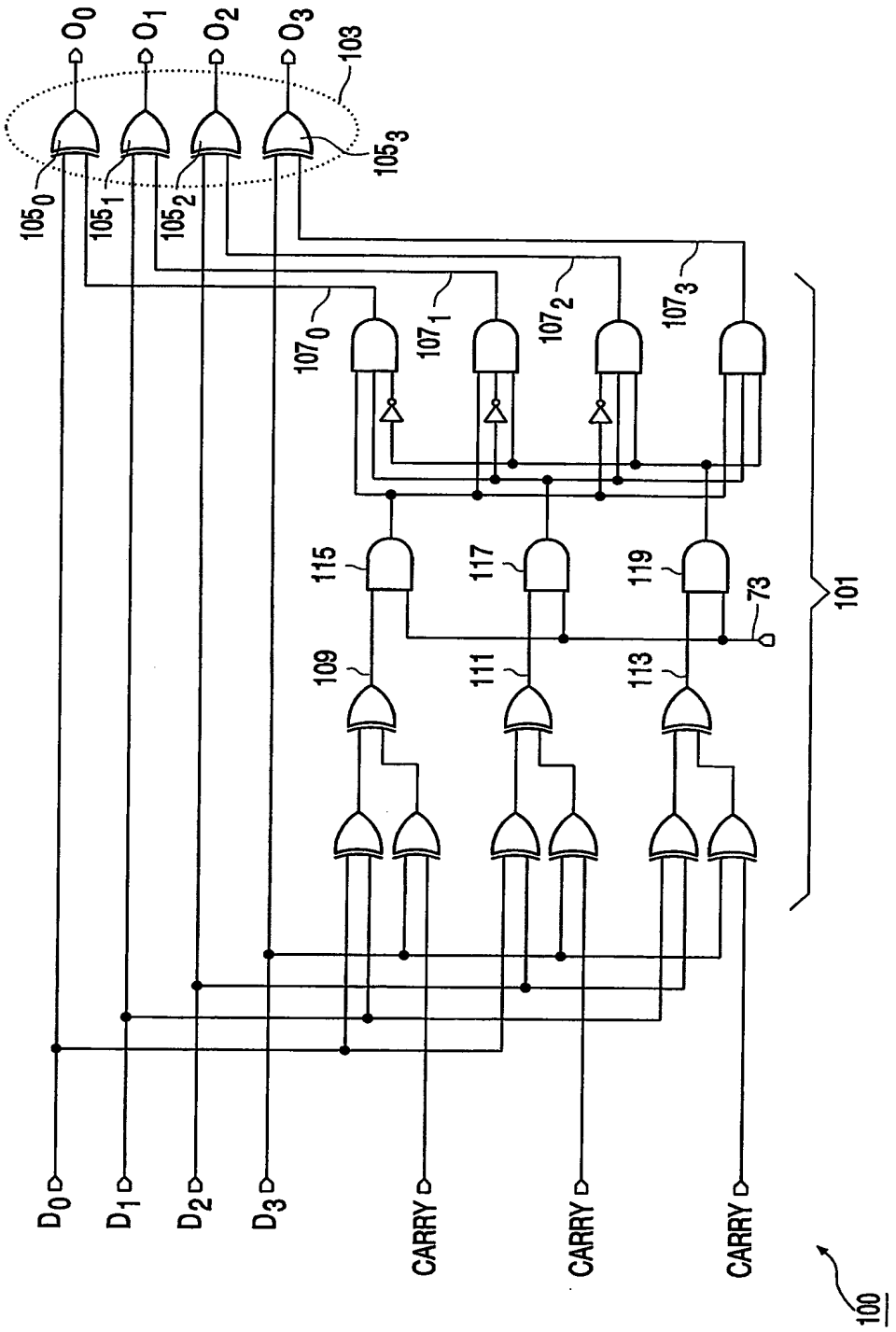
O0
O1
O2
O3
103
1053
1050
1051
1052
1070
1071
1072
1073
115
117
119
73
101
109
111
113
D0
D1
D2
D3
CARRY
CARRY
CARRY
100

FIG. 11